DESCRIPTION

# ACTIVE MATRIX DISPLAY DEVICES

This invention relates to active matrix electro-optic display devices comprising an array of pixels addressed via sets of address conductors, and particularly to active matrix liquid crystal display devices (AMLCDs). The invention is concerned more especially with active matrix display device circuit arrangements and methods of operation for addressing groups of two or more sub-pixels within the array.

Conventionally, AMLCDs comprise a row and column array of pixels which are connected to, and addressed via, sets of row and column address conductors. The pixels of one row are usually connected to the same row address conductor while each pixel in the row is connected to a respective, and different, column address conductor. An example of such a device, its method of operation, and its method of fabrication are described in US-A-5130829 to which reference is invited and whose contents are incorporated herein.

Such display devices are widely used in a variety of products, including for example lap-top computers, PDAs and mobile phones and other portable electronic equipment. Full colour display devices are now becoming more common in relatively small products such as mobile phones. Also, for portability, these products tend to rely on batteries for their power.

It is desirable for display devices intended for use in mobile phone applications and the like to have a very low power consumption in order to conserve battery power. However, there is increasing interest in integrating video functions into mobile devices which means that they must also have good grey scale capability. It is difficult to satisfy both of these requirements at the same time and therefore display devices have been proposed which can be operated in two different modes, a relatively high power, full grey scale, mode and a low power mode which has reduced grey scale capability.

One technique for reducing the power consumption of the display device is to operate it in an 8 colour mode in which the red, green and blue pixels of the display device are driven to one of two states, a light state in which the light transmission, or reflection, of the pixel is high and a dark state in which the light transmission, or reflection, is low. This method of operating the display device offers a reduced power consumption because the circuitry, such as digital to analogue converters, which is required to generate the drive voltages for the grey scales can be put into an inactive, low power, state.

This low power operating mode can be extended to offer increased grey scale and colour capability by dividing the pixels of the display into sub pixels. These sub pixels can be given different areas, for example a pixel may consist of two sub pixels one having an area A and a second having an area 2A. By independently driving these sub pixels to the dark state or the light state the display can be operated to produce 64 colours and 4 grey levels with only a moderate increase in power consumption compared to the 8 colour operation.

Examples of AMLCDs using this area-ratio grey-scale sub-pixellation approach are described, for example, in US 6,335,778 B1 and US 2002/0047822A1, whose contents are incorporated herein as reference material.

Dividing each pixel into a number of sub pixels raises the issue as to how these additional sub pixels should be addressed. Figure 1 illustrates one approach to addressing the additional sub pixels, similar to the kind of approach described in US 2002/0047822A1, in which each sub pixel, P1 to P4, of a pixel P is addressed in a similar way to a conventional pixel. A respective TFT (Thin Film Transistor) is connected between each sub-pixel and a common, adjacent, column address conductor 15 associated with column m of the array. Additional row address conductors 14 are provided, making four in total, Row n to Row n+3, so that each sub pixel can be separately addressed with drive voltages applied to the column conductor. Examples of the row addressing waveforms required are shown in Figure 1a. The address period for the four sub pixels is divided into four sections during each of which a row selection signal is applied to a respective row address

conductor to turn on the associated TFT and simultaneously a data voltage signal is applied to the column address conductor charge the associated sub pixel. A disadvantage of this addressing technique is that the capacitance of the column conductor will be increased by both the capacitance of the additional TFTs connected to it and the capacitance of the crossovers with the additional row conductors. The increased capacitance leads to an increase in power consumption. Other problems, such as the need to use enlarged components in the column drive circuit can also arise.

It is an object of the present invention to provide improved circuit arrangements for the pixels, and methods of operating such, enabling addressing of groups of two or more sub pixels. It is a further object to provide circuit arrangements which are compatible with operation of the display device in a low power stand by mode with reduced colour and grey-scale capability, for example 64 colours, and in a video mode with a full grey scale capability.

In accordance with an aspect of the present invention, there is provided an active matrix display device comprising an array of pixels, a set of row conductors through which rows of pixels are selected, a set of column conductors through which data signals are supplied to selected pixels, each pixel comprising a plurality of sub pixels which sub pixels are each associated with a respective switching transistor for controlling the supply of a data signal to the sub pixel, wherein the plurality of sub pixels of a pixel are coupled to a column conductor associated with the pixel via a common switching transistor through which data signals are supplied to the sub pixels, and wherein the device is operable in a first mode in which the plurality of sub-pixels of a pixel are addressed simultaneously with a data signal and in a second mode in which the sub pixels of a pixel are addressed individually with respective data signals.

The manner in which the sub pixels are connected, with all the sub pixels of a pixel being addressed via one TFT that is connected to the column conductor, has the advantage that the capacitance of the column address conductor is significantly reduced compared to the arrangement of Figure 1.

When the display device is operated in the video mode this common TFT can be used to control the simultaneous charging of the sub pixels. In the low power operating mode the additional TFTs associated with the sub pixels can be used to allow different data to be applied to the sub pixels.

The sub pixels of a pixel may conveniently be connected in a serial or parallel manner.

For ease of controlling the switching transistors and enabling readily the operation of the pixels in the first and second modes, the switching transistors associated with the sub pixels of a pixel are preferably connected to respective, different, row conductors.

The invention is particularly advantageous in relation to AMLCDs, in which the sub pixels comprise liquid crystal display elements, but may be used in active matrix display devices using other kinds of display elements, for example electrophoretic display elements.

These and other advantageous features in accordance with the present invention are illustrated specifically in embodiments of various and different aspects of the invention now to be described, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 shows schematically a possible circuit of a typical pixel, comprising a plurality of sub pixels, in an AMLCD.

Figure 1a shows schematically example waveforms for operating the AMLCD of Figure 1;

Figure 2 shows schematically the circuit configuration of a typical pixel, comprising a plurality of sub pixels, in an embodiment of AMLCD according to the present invention;

Figure 3 shows schematically the circuit configuration of a typical pixel, comprising a plurality of sub pixels, in another embodiment of AMLCD according to the present invention;

Figures 4 and 5 illustrate schematically waveforms used in the driving of the devices of Figures 2 and 3 respectively;

Figure 6 shows schematically, and in highly simplified form, an AMLCD according to the invention;

Figure 7 shows schematically the circuit configuration of part of the pixel array, comprising a plurality of pixels in adjacent rows and columns, in a further embodiment of AMLCD in accordance with the present invention; and

Figures 8 and 9 illustrate schematically waveforms used in the driving of the device of Figure 7 and the effects on the pixels concerned in first and second modes of operation.

The same reference numbers and symbols are used throughout the Figures to denote the same or similar parts.

Referring to Figure 2, there is shown a part of a first embodiment of AMLCD in accordance with the invention, comprising a typical pixel P consisting of a plurality, in this case four, sub pixels, P1-P4, each having an associated TFT switch, T1-T4.

The group of sub pixels constituting the pixel P are connected in a serial manner. Each sub pixel P1 to P4 is connected to the output terminal of a respective TFT switch T1 to T4 with the input terminal of the TFT switches T2 to T4 being connected to the preceding sub pixel. The input of the TFT switch T1 associated with the first sub pixel, P1, is connected to the associated column conductor 15 associated with column m of the array. Data voltage signals for each of the sub pixels P1 – P4 are supplied through this single column conductor and the TFT T1 which for this purpose is common to all sub pixels P1 – P4. Each TFT switch T1 – T4 has a separate switching control (gating) signal which is supplied via a respective, different row conductor 14, Row n – Row n+3, to which its control (gate) electrode is connected.

In the second example embodiment illustrated in Figure 3, the group of sub pixels P1 – P4 of the pixel P are connected in a parallel manner. Again each sub pixel P1 to P4 is connected to the output terminal of a switching TFT T1 – T4 but in this case the input terminals of all TFTs except that associated with the first sub pixel P1 are connected to the first sub pixel, P1. As before each TFT has a separate control signal supplied via a respective and different

row conductor 14, Row n – Row n+3, to which its control (gate) electrode is connected. Again TFT T1 is common to all sub pixels P1 – P4 in that they all receive their data signals through this TFT.

In both example embodiments, the number of sub-pixels in each pixel group can, of course, be varied.

It will be appreciated that for each pixel only one TFT, the common TFT, is connected directly to the column conductor. Consequently, the capacitance of the column conductor is considerably reduced compared with the known arrangement in which each sub pixel TFT is connected to the column conductor.

Both of these pixel circuit configurations have the further advantage that they can readily be addressed in the two modes which correspond to the low power mode and video mode described previously.

In the low power mode of operation different video information must be applied to each of the sub pixels. This is achieved by supplying the information in the form of data voltage signals sequentially to the column conductor and by applying appropriate switching waveforms to the row conductors. The switching waveforms required by the two example circuits of Figures 2 and 3 are different and are illustrated in Figures 4 and 5, respectively.

In the case of the first example embodiment of Figures 2 and 4, the sub pixels P1 – P4 are charged sequentially, starting with P4 and ending with P1. This is achieved by using the overlapping row addressing, (switching), pulses shown in Figure 4 to control the TFTs T1 – T4 appropriately. Each of the TFTs T1-T4 is turned on for a period corresponding to that of the row addressing pulse on its associated row conductor, Row n – Row n+3, allowing the signal present on the column conductor to pass therethrough. As shown, the timings of the row addressing pulses applied to the row conductors Row n – Row n+3 are such that in a first part of a row address period, in which the sub pixels of a row of pixels are all addressed, a data signal applied to the column conductor and intended for sub pixel P4 is transferred through all the TFTs to that sub pixel (and all other sub pixels). At the end of this first period, the TFT T4 is turned off and the data signal is stored on sub pixel P4. In a following period,

a data signal intended for sub pixel P3 is applied which is transferred through TFTs T1 to T3 to that sub pixel and stored thereon at the termination of the row addressing pulse applied to Row n+2. The remaining sub pixels are addressed similar manner in subsequent address intervals with sub pixel P1 being the last to be addressed with its intended data signal. At the termination of the row addressing pulse applied to the row conductor Row n, therefore, each sub pixel is charged according to its relevant data signal.

In the case of the second example embodiment of Figures 3 and 5, the TFT switches T2 to T4 associated with all sub pixels apart from the first are selected sequentially while the first TFT T1 is held in a conducting state. Finally, the first sub pixel P1 is charged and then the first TFT T1 is turned off. The row addressing pulse applied to Row n lasts for substantially all the row address period so as to hold TFT switch T1 on in this period and allowing data signals to be passed to sub pixels P2, P3 and P4 in respective sub-intervals in which the TFTs T2, T3 and T4 are turned on, individually, by appropriate address pulses of their associated row conductors T2, T3 and T4, starting with TFT switch T4 in an initial period.

In the video mode of operation for both embodiments, the same drive, data, voltage signal is applied to all of the sub pixels P1 to P4. This is achieved by holding the associated row conductors, Rows n+1 to n+3, at a voltage which turns on the TFT switches T2 to T4. Row n is then driven with conventional row selection waveforms, the row voltage being switched to a select (gating) voltage level in order to turn on the TFT switch T1 connected to the column conductor and to charge all sub pixels P1 – P4 simultaneously, and then returned to a non-select voltage level in order to turn off this TFT T1 and to isolate the sub pixels P1 – P4 from the column electrode. The TFT switches T2 to T4 of all pixels in the array can be simply held on for the duration of this operational mode.

With regard to both embodiments, the row address pulses applied to the row conductors and the data signals applied to the column conductors and supplied by peripheral drive circuits in generally conventional manner. Figure 6 shows schematically a display device according to the invention and using

pixels of the kind described above with reference to Figures 2 and 3. The pixels P, each comprising a plurality of sub pixels, are organised in rows and columns to form a display pixel array 30. Typically, there may be several hundred rows and columns of pixels. The pixels P in the same row share the same row conductor, 35, each row of pixels thus having four associated row conductors in the case of the above described examples, while the pixels P in the same column share the same column conductor, 38. The pixels are driven by peripheral drive circuitry comprising a row drive circuit 40 connected to the set of row conductors 35 and a column drive circuit 40 connected to the set of column conductors 38, the row and column drive circuits being arranged to provide the required row address pulses and data signals to the row conductors and column conductor associated with a pixel as described above. In a respective row address period the pixels in one row are all addressed at the same time, using common row address pulses applied to their associated sub-set of row conductors 35 and appropriate data signals applied to their respective column conductors 38. Each row of pixels is addressed in sequence in a respective row address period in a frame period and repetitively addressed in similar manner in successive frame periods. The operation of the row and column drive circuits 40 and 42 is controlled and synchronised by a timing and control circuit 45 to which is supplied a video signal VS containing video information from which the data signals required for the sub pixels are derived. The row drive circuit 40 comprises a digital shift register type circuit similar to conventional row drive circuits but suitably modified so as to provide in a row address period the necessary row address pulses to a sub-set of row conductors Row n – Row n+3 when addressing a row of pixels, as described previously with reference to Figure 4 or 5. Likewise, although generally similar to conventional column drive circuits, column drive circuit 42 is appropriately modified to provide data signals to each column conductor 38 in the manner required for the previously described operation of the pixels. In addition, the row and column drive circuits are selectively controllable by the timing and control unit 45 in response to a mode selection control signal MS applied thereto so as to switch the manner of operation of these circuits between that

required for a low power mode of operation of the pixels and that required for a video mode of operation of the pixels as previously discussed. The kind of modifications necessary to the row and column drive circuits for these purposes will be apparent to the skilled person.

As in conventional AMLCDs, the sets of address conductors 35 and 38, the TFTs T1 – T4 of each pixel, and sub pixel electrodes defining the sub pixels P1 – P4 of each pixel are all carried on a first substrate, for example of glass, which is spaced from a second substrate carrying a continuous electrode common to all sub pixels in the array, with liquid crystal disposed between the substrates. Using, for example, low temperature polysilicon thin film technology, the drive circuits 40 and 42 are preferably integrated on the first substrate and fabricated simultaneously with the active matrix circuit of the pixels.

It is possible to reduce the number of row conductors required to address the display device by using a modified pixel circuit and modified row addressing waveforms. An example of part of an array which makes use of the addressing scheme proposed here is shown in Figure 7. In this example pixels X+1 and X+2, X+3 and X+4, X+5 and X+6 etc. represent pairs of sub pixels in a display device which provides for a 64 colour low power operating mode by dividing the area of each pixel into two area ratioed sub pixels.

Considering, for example, the pixel comprising sub pixels x+1 and x+2, the TFT T1 associated with sub pixel x+1 is controlled by row addressing pulses on row conductor Row n while the TFT T2 associated with the sub pixel x+2 is controlled by row addressing pulses on the next row conductor, Row n+1. The input of the TFT T2 is connected to the column conductor Column m while the input of the TFT T1 is connected to the output of TFT T2, whereby a data signal for sub pixel x+2 is supplied via TFT T2 while a data signal for sub pixel x+1 is supplied via both TFTs T2 and T1. The following pixel in the same column, comprising sub pixels x+3 and x+4 is connected in a similar way with TFTs T3 and T4 associated with sub pixel x+3 and x+4 respectively being controlled by row address pulses on row conductors Row n+1 and Row n+2 and with the input of TFT T4 being connected to column conductor Column m

and the input of TFT T3 being connected to the output of TFT T4. The remaining pixels in the same column are connected in similar manner. The pixels in other columns are arranged in corresponding manner, with the pixels in each column being connected to a respective, and different column conductor and with adjacent pairs of pixels each sharing a row conductor.

In the low power mode, where the sub pixels must be addressed with different information, the array is scanned from top to bottom using the row addressing waveforms shown in Figure 8 with the waveform labelled Row n being applied to row conductors Row n and so on. In order to address the sub pixels X+2, X+4, X+6, X+8 etc, the row conductor below the pixel must be taken to a select level. In order to address the sub pixels X+1, X+3, X+5, X+7 etc. both the row conductor above and the row conductor below the pixel must be taken to the select voltage level.

Since taking one of the row conductors to the select voltage level will affect both the row of pixels above and below the selected row conductor it is important that the rows are addressed in the correct sequence so that information applied to a particular sub pixel is not corrupted when a subsequent sub pixel is being addressed.

Figure 8 indicates the operations that are being performed on each of the sub pixels during each period of the addressing sequence. There are three types of operation:

1) Charging, (labelled "Charge Pixels" in Figure 8), when the sub pixel is connected to the column conductor via the switching TFTs and is charged to the voltage present on the column conductor.

2) Charge sharing, (labelled "Share Charge" in Figure 8), when the TFT between a pair of the sub pixels is turned on and charge sharing takes place between the capacitances of the sub pixels, the sub pixels being isolated from the column conductor during this operation.

3) Holding, (labelled "Hold Voltage" in Figure 8) when the voltage is maintained on the capacitance of the sub pixels.

As shown in Figure 8, in a first sub-period of the illustrated addressing cycle row address pulses are applied to row conductors Row n and Row n + 1

thereby turning on TFTs, T1, T2 and T3. At the same time a data signal voltage intended for sub pixel x+1 is applied to the column conductor column m, thus charging sub pixels x+1 and x+2. Because TFT T3 is also turned on in this sub-period, charge sharing occurs between sub pixels x+3 and x+4. In the following sub-period, the row address pulse on row conductor Row n only is maintained while a data signal intended for a preceding sub pixel x (not shown) is applied. During this sub-period the voltages on sub-pixels x+1 and x+2 are held. In the next sub-period the row address pulse on Row n is removed and row address pulses applied to Row n + 1 and Row n + 2, with a data signal intended for sub pixel x+3 applied to the column conductor. This results in the voltage on sub pixel x+1 being held while the sub pixel x+2 is charged to this data signal level. At the same time charging of sub pixels x + 3 and x + 4 takes place while charge sharing between sub pixels x + 5 and x + 6 occurs. In the next sub-period the row address pulse on Row n + 2 is removed while the row address pulse on Row N + 1 is maintained. In this sub-period a data signal intended for sub pixel x + 2 is applied to the column conductor. Thus, the voltage on sub pixel x + 1 is still held while sub pixel x + 2 is charged to the data signal level, and the voltage on sub pixels x + 3 and x + 4 is merely held. In the following sub-period, in which a data signal intended for sub pixel x + 5 is applied to the column conductor, the address pulse on Row n + 1 is removed, and address pulses applied to Row n + 2 and Row n + 3. This results in the voltages on sub pixels x + 1, x + 2 and x + 3 being held, the charging of sub pixels x + 4, x + 5 and x + 6, and charge sharing between sub pixels x + 7 and x + 8.

This manner of operation continues, as depicted in Figure 8, until all the sub pixels in the column have been charged according to their intended data signals.

While Figure 8 shows the manner in which the pixels in one column are addressed, it will be appreciated that the other columns of pixels are addressed in a similar way and at the same time.

The sequence in which the sub pixels are addressed is chosen so that after a sub pixel has been charged to the required drive voltage level,

according to the supplied data signal voltage, it will not undergo any further charge sharing or charging operation until shortly before it is re-addressed in the following field period.

In the video operating mode the same video information must be applied to pairs of sub pixels. This is achieved using the addressing waveforms shown in Figure 9. In this mode, the display device must be scanned in the reverse direction, from bottom to top, in order to avoid disturbing the pixel voltage after it has been addressed. Thus in a first sub-period of the illustrated addressing cycle, row address pulses are applied to Row n + 3 and Row n + 4 while a data signal voltage for sub pixels x + 7 and x + 8 is applied to the column conductor. Consequently, sub pixels x + 6, x + 7 and x + 8 are all charged to the level of this data signal while the voltage on all other sub pixels in the column is held. In a following sub-period, a data signal intended for sub pixels x + 5 and x + 6 is applied and row address pulses applied only to Row n + 3 and Row n + 2, resulting in the voltage on sub pixels x + 7 and x + 8 being held, and sub pixels x + 4, x + 5 and x + 6 being charged to the applied data signal level. This manner of operation continues, as depicted in Figure 9, until all sub pixels have been addressed.

While described in relation to AMLCDs in particular, it is envisaged that the invention may be applied to active matrix display devices using electro-optic materials other than LC material, for example electrophoretic material.

In summary, therefore, active matrix display devices have been described which have an array of pixels addressed via sets of row and column conductors to which, respectively, selection and data signals are applied, each pixel comprises a plurality of sub pixels which each have an associated switch, for example a TFT, (T1 – T4) and which are addressed with data signals through a common switch (T1) coupled to a column conductor. Addressing the sub pixels through a common switch reduces the effective capacitance of the column conductor.

By appropriate control of the switches (T1 – T4) the pixels can be driven in a first mode in which the common switch (T1) is operated to control the simultaneous addressing of the sub pixels (P1 – P4) with a data signal, for

example, for a video display with full grey scale capability, and in a second mode in which the switches (T1 – T4) are controlled sequentially to allow different data signals to be applied to the individual sub pixels, for example, as required for a low power standby mode of operation with limited grey scale and colour capability.

From reading the present disclosure, many other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the art and which may be used instead of or in addition to features already described herein.